IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

INNOVATIVE FOUNDRY TECHNOLOGIES LLC,

Plaintiff,

v.

SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION; SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION; SEMICONDUCTOR MANUFACTURING INTERNATIONAL (BEIJING) CORPORATION; SEMICONDUCTOR MANUFACTURING INTERNATIONAL (TIANJIN) CORPORATION; SEMICONDUCTOR MANUFACTURING INTERNATIONAL (BVI) CORPORATION; SEMICONDUCTOR MANUFACTURING NORTH CHINA (BEIJING) CORPORATION; SEMICONDUCTOR MANUFACTURING SOUTH CHINA CORPORATION; BROADCOM INCORPORATED; BROADCOM CORPORATION; CYPRESS SEMICONDUCTOR CORPORATION; and DISH NETWORK CORPORATION.

Defendants.

C.A. No.: 6:19-cv-00719-ADA

JURY TRIAL DEMANDED

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS

Exhibit S	S. Wolf & R.N. Tauber, *Silicon Processing for the VLSI Era - Vol. I - Process Technology*, pp. 194-195 (2nd ed., 2000)
Exhibit T	Jerry Ruzyllo, *Semiconductor Glossary*, p. 24 (2004)

LIST OF COMMON ABBREVIATIONS

'126 patent	Asserted U.S. Patent No. 6,806,126
'620 patent	Asserted U.S. Patent No. 6,933,620
'122 patent	Asserted U.S. Patent No. 6,580,122
'226 patent	Asserted U.S. Patent No. 7,009,226
IFT	Plaintiff Innovative Foundry Technologies LL
Defendants	Defendants Semiconductor Manufacturing International Corporation;[1] Semiconductor Manufacturing International (Shanghai) Corporation; Semiconductor Manufacturing International (Beijing) Corporation; Semiconductor Manufacturing International (Tianjin) Corporation; Semiconductor Manufacturing International (BVI) Corporation; Semiconductor Manufacturing North China (Beijing) Corporation; Semiconductor Manufacturing South China Corporation; Broadcom Incorporated; Broadcom Corporation; Cypress Semiconductor Corporation; and Dish Network Corporation
PH	prosecution history
STI	shallow trench isolation

NOTE: All emphases in this brief have been added, unless otherwise noted.

[1] Defendant Semiconductor Manufacturing International Corporation ("SMIC Cayman") is a foreign holding company that contests personal jurisdiction in this matter and has moved to dismiss on that basis. *See* ECF No. 68. Semiconductor Manufacturing International (BVI) Corporation ("SCMI BVI") has also moved to dismiss. *See* ECF No. 98. The other named Defendants, apart from Defendants Cypress Semiconductor Corporation, Broadcom Incorporated, Broadcom Corporation, and DISH Network Corporation, have not yet answered the amended complaint. By submitting this document, SMIC Cayman and SMIC BVI do not waive the arguments in their pending motions to dismiss, nor do any of the Defendants which have not yet answered waive any Rule 12 arguments or motions they may bring.

I. INTRODUCTION AND SUMMARY OF ARGUMENTS

Although the parties agree on the meaning of the term "silicide," they dispute the construction of four terms spread across the four patents-in-suit and whether two terms in certain claims of the '126 patent are indefinite.

"Recessed isolation structure" in the '122 patent: The Court should construe the term "recessed isolation structure" as "an isolation structure whose uppermost surface is positioned below the substrate's uppermost surface." IFT's "plain and ordinary meaning" approach does not resolve the parties' dispute because "recessed isolation structure" is a coined term that simply lacks an established plain and ordinary meaning. This is evidenced by IFT's own infringement contentions, which go well beyond what could be understood from the intrinsic evidence as a "recessed isolation structure." The intrinsic evidence fully supports Defendants' construction, with language in the claims stating the specific depth at which the isolation structure's surface is positioned below the substrate's surface. Ex. A ('122 pat.) at cls. 4, 15, 26. The same express teaching appears in the specification. *Id.* at 4:42-49. Figures 6 and 7 of the '122 patent, which depict the "present invention" rather than just embodiments of the invention, also show a recessed isolation structure (34) with a top surface well below the top surface of the substrate (30), resulting in a recess (49) defined by the substrate's sidewalls on the sides and the recessed isolation structure below. *Id*. at Figs. 6A-B, 7A-C. Only Defendant's construction comports with the intrinsic record and avoids a nonsensical interpretation that essentially reads "recessed" out of the claims.

The Order of Steps of Independent Method Claim 1 in the '126 patent: The Court should construe asserted independent claim 1 of the '126 patent as requiring its steps to be completed in the order written. "Plain and ordinary meaning," as IFT proposes, is legally inadequate because an order-of-step dispute is a claim construction issue for the Court rather than a jury. *See Moba v. Diamond Automation*, 325 F.3d 1306, 1313 (Fed. Cir. 2003). Here, the steps

of claim 1 refer to structures "provid[ed]" or "form[ed]" in prior steps, thus requiring a sequence as a matter of grammar and logic. Further, semiconductor manufacturing involves an incremental process in which each step builds upon the prior steps, so that the technology itself calls for the steps to be performed in the claimed order. *See Nitride Semiconductors Co. v. RayVio Corp*., 2018 WL 2183270, at *4 (N.D. Cal. May 11, 2018). And the specification fully supports this sequential requirement by only describing the performance of steps in the claimed sequence. *See Mantech Envtl. Corp. v. Hudson Envtl. Servs., Inc*., 152 F.3d 1368, 1376 (Fed. Cir. 1998).

"Adjacent" in the '126 and '620 patents: The parties disagree about the plain and ordinary meaning of "adjacent" which appears in these two related patents. According to the term's common meaning, Defendants submit that two items are "adjacent" when these items are relatively near to each other and have nothing of the same kind intervening. Although IFT disagrees, it refuses to articulate its understanding of the term's plain meaning, probably to better conceal its position that two nitride spacers would be "adjacent" despite having a third spacer of a different material between them. Under IFT's strained argument, Texas would be "adjacent" to Mississippi despite having the intervening state of Louisiana and nearly 300 miles in between. By contrast, according to the term's common meaning, Louisiana (a state) is adjacent to Texas (a state), despite having the Sabine River (a river) between them. This common meaning of "adjacent" is consistent with the specification's use of the term when describing the positional relationship between structures. *Compare, e.g.*, Ex. B ('126 pat.) at 2:28-29 & 3:52-54 (describing nitride spacer and sidewall as adjacent where the intervening structure is an oxide layer), *with* 1:41-43 (*not* describing nitride spacer and sidewall as adjacent where intervening structure is an oxide *spacer*; nitride spacer is instead described as adjacent to oxide spacer). What's more, the term's common meaning advances the patent's purported advantage described in the specification and

emphasized during prosecution to overcome prior art rejections, while IFT's "anything goes" position allowing intervening structure of the same kind undermines it. *Id*. at 6:13-17; *see* Part IV.C.4, *infra*. The Court should resolve this dispute by adopting Defendant's proposal.

"Conformal" in the '226 patent: The Court should construe "conformal" to mean "having a uniform thickness and following the contours of the layer below." Although the parties agree that this term needs a construction, they disagree on whether the meaning of this term requires a uniform thickness. The intrinsic evidence confirms that it does. The prior art considered during prosecution (thus qualifying as intrinsic evidence), and sharing a common inventor with the '226 patent, expressly indicates that "conformal" is understood in the art to require equal thickness throughout: "Another desired characteristic for interlevel dielectrics used in interconnect formation is ***conformality***, such that ***film thickness is equal over all substrate topography***." Ex. E ('217 pat.) at 2:11-14. Objective extrinsic evidence, like textbooks, treatises, and technical dictionaries published before the filing of the '226 patent confirm this ordinary meaning of "conformal" in this field. For example, a textbook from 2000 defines "conformal coverage" as "a condition where ***equal film thickness*** exists over all substrate topography[,]" while a technical glossary from 2004 defines "conformal coating" as a "deposited film which ***thickness remains the same*** regardless of underlying geometrical features." Consistent with this ordinary meaning in the art, the'226 patent describes and depicts the "conformal" layers as having the same thickness throughout, while non-conformal layers in the patent have varying thicknesses. The Court should adopt this ordinary meaning of "conformal" to a skilled artisan in this field.

Indefinite terms of the '126 patent: The term "***the portions*** of the semiconductor material ***adjacent the gate structure***" in claim 6 of the '126 patent is indefinite for lack of antecedent basis. The only prior recitation of "portions" in any claim is "portions of the first and second ***sides of the***

gate structure," which cannot provide antecedent basis lest the portions in claim 6 become adjacent to themselves. The term "***the*** first and second sidewalls" in claim 8 is also indefinite for lack of antecedent basis because no claim on which claim 8 depends uses the term "sidewall" or even "wall." Accordingly, these terms and their respective claims are indefinite.[2]

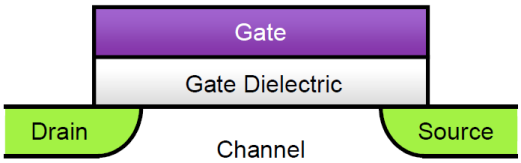
II. AGREED-UPON CONSTRUCTION

Defendants and IFT have agreed to construe the term "silicide," which appears in the '126 and '620 patents, to mean "silicide, salicide and/or polysilicide." Defendants respectfully request that the Court adopt this agreed-upon construction.

III. CLAIM CONSTRUCTION DISPUTE FOR THE '122 PATENT

A. Relevant Technology Background

As its title indicates, the '122 patent generally relates to transistors. Ex. A ('122 pat.). Semiconductor transistors normally comprise a gate isolated from the substrate by a gate dielectric material (*e.g.*, silicon oxide), and source/drain terminals formed in the substrate. The inset diagram provides a conceptual depiction of the well-known structure of a transistor. When a voltage is applied to the gate (*e.g.*, via a gate electrode), a conducting channel forms in the substrate and allows current to flow between the source and drain.



The '122 patent provides an example of a prior art transistor in its Figure 1, shown in the inset below. *Id.* at Fig. 1 (colors and labels added). This prior art transistor (10), which is formed in an active area (12), comprises a gate electrode (20) isolated from the substrate (14) by a gate insulation layer (18), and includes source and drain regions (28) formed in the substrate on either

[2] Because the Court is already very familiar with the precedent governing claim construction and indefiniteness, Defendants omit an overly long recitation of such precedent in this brief and, instead, cite applicable authorities where appropriate in their analysis of each disputed term.

side of the gate electrode. *Id.* at 1:38-43. The channel between the source and drain is labeled with a "L" in Figure 1. *Id.* at 1:34-37. To ensure proper operation, the active area (12) is electrically isolated from other active areas by isolation structures (16) formed in the substrate. *Id.*

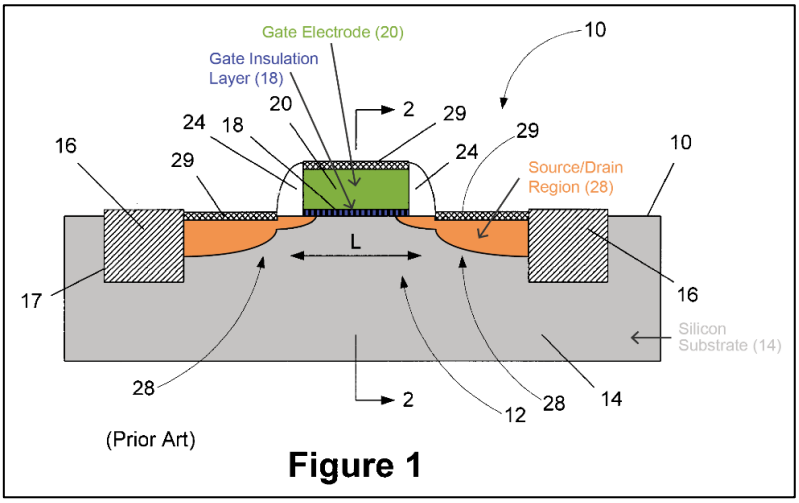


Figure 1

An isolation structure in wide use before the filing of the '122 patent was a shallow trench isolation ("STI") structure. *Id.* at 1:55-57. Construction of an STI involves digging a trench (17) in the substrate (14), filling the trench with insulating material (16) such as silicon dioxide, and then performing a polishing operation to remove excess insulating material. *Id.* at 1:57-61.

As the '122 patent's Background section explains, it was important to maximize the transistor's "drive current," which is "the amount of current flowing from the drain region to the source region of a transistor." *Id.* at 1:62-2:4. Drive current can be improved by either reducing the transistor's channel length "L" or increasing the transistor's channel width "W". *Id.* at 2:5-20; *see also id.* at 1:36-38 (explaining that W corresponds to the cross-section of Fig. 1's transistor along the line 2—2). But these two approaches increased undesirable leakage current when the transistor is turned off. *Id.* at 2:5-20. Because an increase in W causes less leakage than a decrease in L, *id.*, the patent expresses a desire "to have a transistor in which the width dimension of a substrate can be maximized in a given plot space of semiconducting substrate." *Id.* at 2:35-38. The '122 patent purports to maximize a transistor's effective width by teaching a transistor with a "recessed" isolation structure. *See, e.g., id.* at 2:43-59.

The '122 patent depicts this claimed transistor in Figures 3 through 7C at various stages of the fabrication process. Figure 6B is a cross-section view of the device along the width W dimension after the formation of gate electrode (42) and gate insulation layer (40) on the substrate (30). *Id.* at 5:33-45, 6:62-7:3. Figure 6B shows recessed isolation structures (34) composed of insulating material in trenches (32), with the recess portions (49, surrounded by red dashed lines) depicted as the space which is above recessed isolation structures (34) and which is delineated by the trench's sidewalls. *Id.* at 4:21-56, 5:58-63; 7:45-55. Figure 6B further shows the gate insulation layer (40) and gate electrode (42) extending down into the recessed portion (49) above the recessed isolation structure (34). *Id.* at 7:45-55.

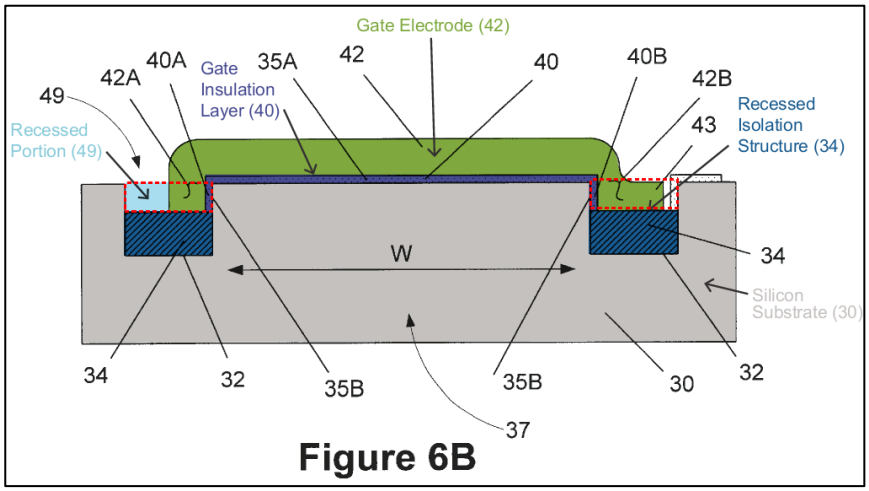


Figure 6B

The '122 patent was filed on March 20, 2001, and issued on June 17, 2003. *Id.* at cover. The three independent claims all recite the term "recessed isolation structure." *Id.* at cls. 1, 13, 23.

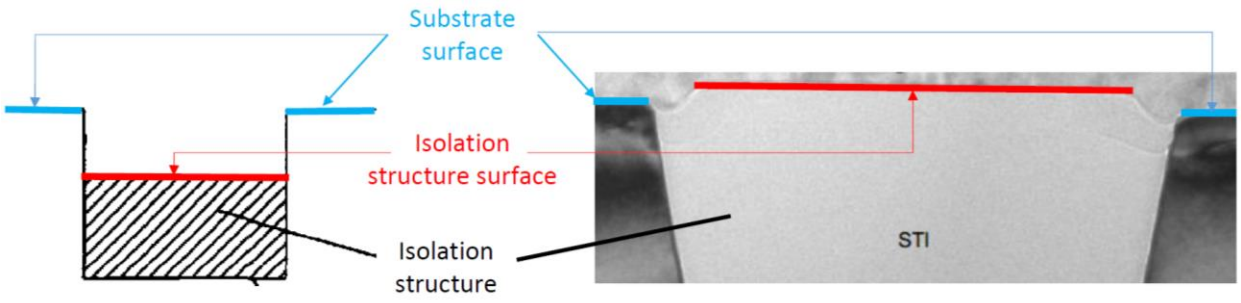
B. "recessed isolation structure" (cls. 1, 3, 5, 12-14, 16, 22-23, 25, 27, 33, 34 of the '122 pat.)

Defendants' Proposed Construction	IFT's Proposed Construction
an isolation structure whose uppermost surface is positioned below the substrate's uppermost surface	plain and ordinary meaning

1. The Court Should Resolve the Dispute about the Term's Scope

Although IFT hides behind an unexplained "plain and ordinary meaning," the parties have a fundamental dispute about the claims' scope. In its infringement contentions, IFT relies on the image below (on right) showing an STI (light gray) whose top surface is ***above*** the top surface of

the substrate (dark gray on either side of the STI). Ex. F (Apr. 1, 2020 Infring. Cont. Ex. 1) at 11. IFT's litigation position contradicts the intrinsic evidence (such as Figure 6A, shown below on left), which requires the isolation structure's top surface to be ***below*** the substrate's top surface.



'122 pat. at Fig. 6A (excerpt)

IFT Infring. Contentions's Ex. 1 at 11 (excerpt)

Compare Ex. A ('122 pat.) at Fig. 6A (excerpt), *with* Ex. F (Apr. 1, 2020 Infring. Cont. Ex. 1) at 11 (labels and color lines added). IFT's position essentially eliminates the word "recessed" from this claim term, while Defendants' proposal give meaning to "recessed."

IFT's proposed "plain and ordinary meaning" cannot resolve this dispute because there is no evidence that "recessed isolation structure" had a technical meaning in 2001 outside of the '122 patent. This is apparent from IFT's inability to articulate what this meaning is and from contemporaneous technical glossaries and textbooks which lack an entry for this term. *E.g.* Ex. G (Quirk & Serda) at 641; Ex. H (Van Zant) at 512-13. Instead, the patentee coined this term to describe the isolation structure used in its alleged invention. *See Iridescent Networks, Inc. v. AT&T Mobility, LLC*, 933 F.3d 1345, 1351-53 (Fed. Cir. 2019) (finding "high quality of service connection" to be a "coined" term and affirming construction limiting the term to the minimum parameters disclosed in the specification). Because there is no "plain and ordinary meaning" for this coined term, the Court should construe this term to assist and guide the jury.

2. The Intrinsic Evidence Defines a Recessed Isolation Structure Based on Its Top Surface Being Below the Substrate's Top Surface

The intrinsic evidence consistently, repeatedly, and exclusively indicates that a recessed isolation structure must have its top surface positioned below the top surface of the substrate.

Indeed, the patent expressly defines "the present invention" in terms of this configuration. Figures 6A-6B and 7A-7C depict the claimed recessed isolation structure (34, shown in striated navy blue) inside trench (32), clearly showing that the isolation structure's top surface is beneath the top surface of the substrate (30, in gray). *E.g.*, Ex. A ('122 pat.) at Figs. 6A-6B & 7A-7C. For example, Figure 7A depicts the portion of the isolation material that was etched away as a recess (49, in light blue). *Id.* at Fig. 7A (colors and labels added); *see also id.* at Figs. 6A-6B & 7B (showing recess (49) above the recessed isolation structure 34). These depictions are critical because, as the patent makes clear, Figures 6A-6B and 7A-7B show the invention: "***As shown in FIGS. 6A, 6B and 7A-7C, the present invention*** is directed to a novel transistor structure." *Id.* at 6:62-63. Hence, Figures 6 and 7 define and depict the claimed invention as having a recessed isolation structure with an uppermost surface below that of the substrate. *See, e.g.*, *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the "present invention" as a whole, this description limits the scope of the invention."); *see also Secure Web Conference Corp. v. Microsoft Corp.*, 640 F. App'x 910, 915 (Fed. Cir. 2016) (affirming ruling that "Figures 1 and 2 depict the essence of the claimed invention rather than a preferred embodiment" and adopting district court's

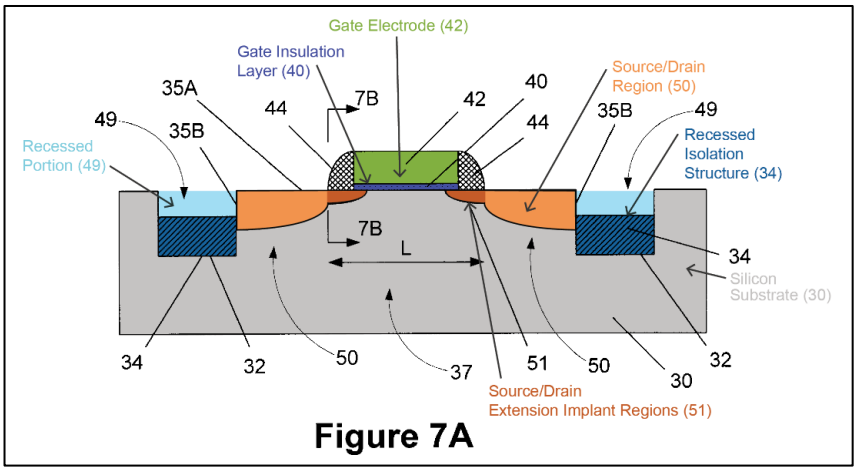


Figure 7A

construction, where the patent described Figures 1 and 2 as the "present invention"). The '122 patent does not depict, disclose, or even hint at a "recessed isolation structure" whose uppermost surface is not actually "recessed" with respect to the substrate.

The claims are consistent with the patent's characterization of its "present invention," by indicating the relative position of the top surfaces of the substrate and isolation structure. The dependent claims, for example, add specific dimensions requiring that "said recessed isolation structure ***has a surface that is positioned*** approximately 1000-1500 Å ***below a surface of said substrate***." Ex. A ('122 pat.) at cls. 4, 15, 26. As the patent makes clear, this claimed surface corresponds to the top "surface 36 of the [recessed] isolation material 34 in the trench 32 [that] is positioned approximately 1000-1500 Å beneath the [top] surface 35 of the substrate 30."[3] *Id.* at 4:45-49; *see also id.* at Fig. 3 (showing top surface 35 of substrate, and top surface 36 of recessed isolation structure 34).

The disclosed technique for forming the recessed isolation structure in this patent similarly supports Defendants' proposed construction of the term. *See, id.* at 4:34-35 ("The recessed isolation material 34 may be formed in the trench by a variety of techniques."). This technique involves first depositing the insulating material into the trench 32 along with a polishing step "such that the insulating material in the trench 32 is approximately planar (not shown) with the surface 35 of the substrate 30." *Id.* at 4:38-42. As a result of this polishing, the top surface of the insulation material and the top surface of the substrate are initially at the same level. Then "[a]n etching process may then be performed to ***reduce the level of insulating material 34 in the trench*** to the level depicted in Fig. 3." *Id.* at 4:42-45. For example, the patent describes removing the insulation

[3] The '122 patent uses the term "recessed isolation material 34" and "recessed isolation structure 34" interchangeably. *Compare, e.g.*, Ex. A ('122 pat.) at 4:34, *with id.* at 7:36.

material, via an etching process, until its top surface is positioned about 1000-1500 Å below the substrate's top surface. *Id.* at 4:45-49 ("[T]he insulating material 34 is ***removed until such time as a surface 36*** of the isolation material 34 in the trench 32 ***is positioned*** approximately 1000-1500 Å ***beneath the surface 35 of the substrate 30***." *Id.* at 4:45-49. The patent thus supports Defendants' proposal.

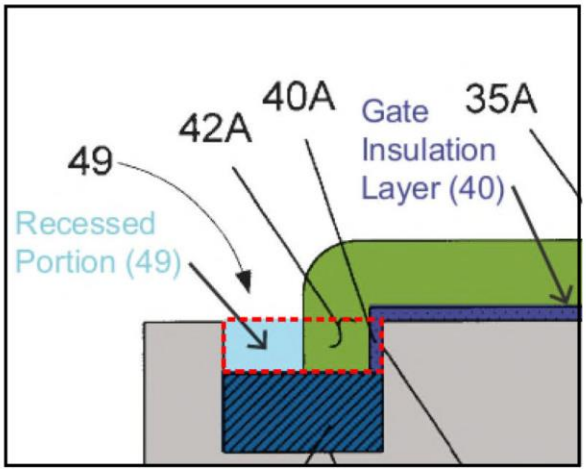
3. Defendants' Construction Avoids Rendering the Claims Nonsensical

The isolation structure's top surface must be below the substrate's top surface for the claims to make sense.

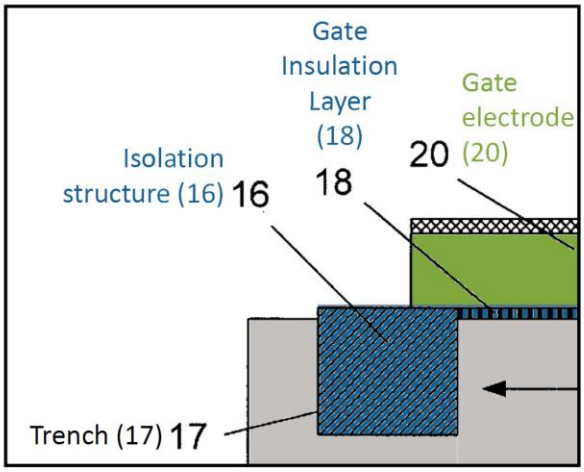
First, independent claims 1 and 13 require that the recessed isolation structure be "formed ***in*** said substrate" and that it "defin[es] a recess ***thereabove***." Ex. A ('122 pat.) at cls. 1 & 13. Per this language, the recess must be formed above the recessed isolation structure. But IFT's position would render this language superfluous by allowing the isolation structure's top surface to be above the substrate's top surface, making it impossible to "define a recess thereabove." As the admitted prior art's isolation structure (16) shows, there is no substrate sidewall to "defin[e] a recess thereabove" once an isolation structure's top surface is higher than the substrate's. *Id.* at Figs. 1 & 2 (labeled as "prior art" and showing isolation structure (16)). For a recess to be above the isolation structure, the structure's top surface must be below the substrate's top surface, as shown by recess (49) in Figures 6-7 (see next page) which reflect the "present invention."

Second, all three independent claims mandate that the gate electrode and the gate insulation extend into the recess. Claims 1 and 13 require that the gate's electrode and insulation layer be "formed above said substrate," with portions of the electrode and insulation layer "extending into said recess above said recessed isolation structure." *Id.* at cls. 1 & 13. While phrased differently, claim 23 calls for the gate's electrode and insulation layer to be "positioned above a portion of said upper surface" of the substrate's active area region, while also extending above the active area's

sidewalls which are below the substrate's surface. *Id.* at cl. 23; *see also id.* at 6:65-7:1 & Figs. 6-7 (describing and showing sidewalls (35) of the active area as being below the substrate's surface). The specification similarly describes the claimed "novel transistor structure" as having "a portion of the gate electrode 42 and the gate insulation layer 40 [that] ***extends downwardly into a recess 49 in the substrate*** above a recessed isolation structure 34." *Id.* at 7:11-15; *see also id.* at Figs. 6B & 7B (showing gate electrode (42) and insulation layer (40) extending down into recess 49). It would be physically impossible for the gate's electrode and insulation layer to satisfy the claim language if the top surface of the recessed isolation structure were above the substrate's top surface as IFT's position permits. *See, e.g., id.* at Fig. 2 (prior art showing isolation structure's top surface above substrate's surface). The following comparison shows the gate electrode (42) and insulation layer (40) in Figure 6B extending down into the recessed portion (49), while the gate electrode (20) and insulation layer (18) in prior art Figure 2 cannot extend into any recess because the isolation structure's top surface is above the substrate's surface:



122 Pat. at Fig. 6B



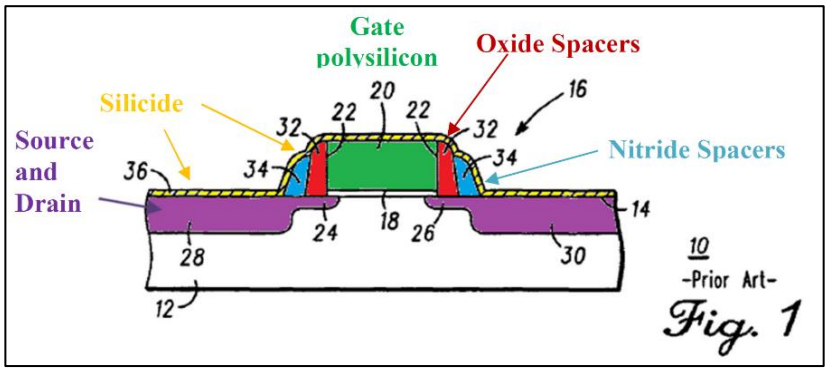
122 Pat. at Fig. 2

Because IFT's position would render the claims facially nonsensical and result in "a physical impossibility," it cannot be correct. *Becton, Dickinson and Co. v. Tyco Healthcare Group, LP*, 616 F.3d 1249, 1255 (Fed. Cir. 2010).

IV. CLAIM CONSTRUCTION DISPUTES FOR THE '126 AND '620 PATENTS

A. Relevant Technology Background

The '126 and '620 patents (the "Luning patents") are related, with the '620 patent being a divisional of the '126 patent and sharing a common specification. These two patents relate "to semiconductor components, more particularly, to the gate resistance of semiconductor components." Ex. B ('126 pat.) at 1:5-7.[4] Such resistance can be reduced by forming silicide on top of the gate polysilicon. *Id.* at 1:30-33. But as manufacturers "shrink the sizes of devices," *id.* at 1:13, this shrinking impairs the formation of silicide, *id.* at 1:29-31, because there is less surface at the top of the gate polysilicon. In particular, spacers "limit[s] formation of silicide to [the gate's] top surface." *Id.* at 1:53-55. Despite this drawback, spacers are necessary to block ion implantation in certain locations and thus to create offsets away from the gate for doped regions like the source or drain regions. For example, the patents' Background section describes a series of an oxide spacer (32) and a nitride spacer (34) on either side of the gate polysilicon. *Id.* at 1:41-43, Fig. 1 (color and labels added). "Oxide spacers 32 offset … the source and drain extension regions 24 and 26," while "[n]itride spacers 34 offset the deep source and drain regions 28 and 30." *Id.* at 1:43-46.



To "allow[] sufficient silicide formation so that the gate resistance remains low," *id.* at 1:59-63, the Luning patents disclose a semiconductor component, along with a method to manufacture this device, that uses "first and second nitride spacers" (118), instead of the prior art's

[4] For brevity, Defendants primarily cite to the specification of the '126 patent where the disclosures are identical, with the understanding that the same passages appear in the '620 patent.

oxide spacers, adjacent the first and second sides (115, 117) of the gate polysilicon (108A), as well as third and fourth nitride spacers (128) adjacent these first two spacers respectively. *Id.* at 2:7-16, Fig. 7 (colors and labels added). The pair of nitride spacers on either side of the gate polysilicon are overetched to expose the top portions of the first and second sides and the top surface of the gate polysilicon. *Id.* at 2:16-18, 2:28-33. Silicide (140) is then formed along the portions of the gate polysilicon's top and sides that are not covered by the spacers, so that "the gate resistance is lowered." *Id.* at 2:21-24, 2:36-38. Silicide (142, 144) is also formed on the source and drain regions (132, 134).

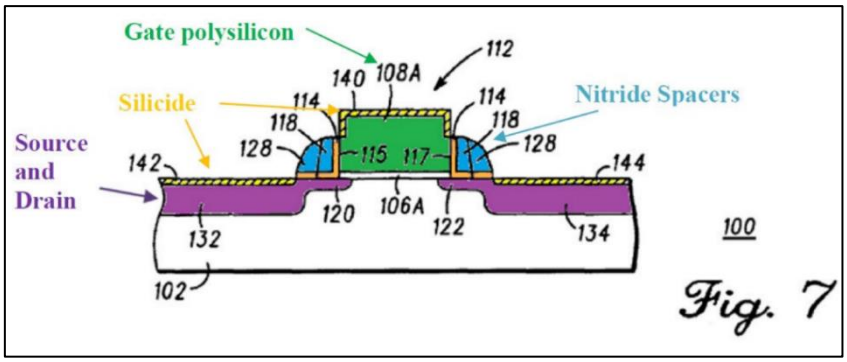


Fig. 7

The '126 patent was filed on September 6, 2002, and issued on October 19, 2005. *Id.* at cover. In response to Defendants' IPR petition against this patent, IFT submitted a statutory disclaimer of claims 12-19, leaving only claims 1-11 as the remaining asserted claims. Ex. I (Jul. 22, 2020 Disclaimer under 37 C.F.R. § 1.321(a)).

The '620 patent was filed on August 9, 2004, and issued on August 23, 2005. Ex. C ('620 pat.) at cover. Claims 1, 7, and 14 are the three independent claims in the '620 patent. In response to Defendants' IPR petition against the '620 patent, IFT submitted a statutory disclaimer of claims 7, 12-17, and 20, leaving only claims 1-6, 8-11, and 18-19 as the surviving asserted claims. Ex. J (Jul. 21, 2020 Disclaimer under 37 C.F.R. § 1.321(a)).

B. The Order of Steps of Independent Method Claim 1 of '126 Patent

Defendants' Proposed Construction	IFT's Proposed Construction
The steps of the claims must be performed in the order written	plain and ordinary meaning

1. A Construction Is Necessary to Resolve the Parties' Dispute

All of the claims of the '126 patent are method-of-manufacturing claims. Although the steps of a method claim do not normally need to be performed in the recited order, the Federal Circuit has held that, where required by the intrinsic evidence, the recited order is limiting and the steps must be performed in that order. *E.g.*, *Mformation Techs., Inc. v. Research In Motion Ltd.*, 764 F.3d 1392, 1398-1399 (Fed. Cir. 2014). As discussed below, the intrinsic evidence mandates following the recited order of steps.

It is clear that IFT disagrees, and it proposes instead to leave this complex legal issue to the jury under the guise of "plain and ordinary meaning." This is an invitation to error, because deciding whether method steps must occur in the recited order is a question of claim scope that is reserved for the Court. *See Moba*, 325 F.3d at 1313 (criticizing district court's failure to resolve whether method claim required sequential performance); *Core Optical Techs., LLC v. Ciena Corp.*, 2013 WL 8719137, at *16-17 (C.D. Cal. Oct. 25, 2013) (rejecting patentee's argument that a jury can decide "whether there is an imposed order" of step, because "it is the Court's duty to resolve" the dispute). The Court should resolve this order-of-steps dispute.

2. As a Matter of Grammar, the Steps of the Claims Must Be Performed in the Order Written

The steps in a method claim must be performed in the recited sequence where an individual step must be completed before the next step begins. *Mformation*, 764 F.3d at 1400 (affirming order-of-step requirement where, "other sub-steps in claim 1 inherently require an order-of-steps. As a matter of logic, a mailbox must be established before the contents of said mailbox can be transmitted"); *E-Pass Techs., Inc. v. 3Com Corp*, 473 F.3d 1213, 1222 (Fed. Cir. 2007) ("Substantively, because the language of most of the steps of its method claim refer to the completed results of the prior step, E-Pass must show that all of those steps were performed in

order."). As in *Mformation* and *E-Pass*, each step of claim 1 builds on each other and requires completion of the prior ones. This requirement is not surprising in a method of manufacture claim and is apparent from the plain language of claim 1, where each of the seven recited steps builds upon the previous one:

- Step 1 before Step 2: Step 1 involves "***providing*** a semiconductor material … ***having a major surface***." Ex. B ('126 pat.) at 6:36-37 (cl. 1). Step 2 then requires "forming a gate structure ***on the major surface***." *Id.* at 6:38. The major surface must exist before a gate structure can be formed on it.

- Step 2 before Step 3: Step 2 includes "forming … the gate structure having ***first and second sides***," while Step 3 calls for "forming first and second spacers ***adjacent the first and second sides*** of the gate structure." *Id.* at 6:40 & 6:42-43. The first and second spacers which are adjacent the gate polysilicon's sides cannot be formed until there is a gate structure with a first and second sides.

- Step 3 before Step 4: Step 3 requires "forming ***first and second spacers***," and Step 4 recites "forming … source extension region ***aligned to the first spacer*** and the drain extension region ***aligned to the second spacer***." *Id.* at 6:42, 6:46-49. As a matter of logic, the extension regions formed in Step 4 cannot be aligned to the spacers until those spacers are formed in Step 3.

- Step 4 before Step 5: As indicated above, the extension regions formed in Step 4 are aligned to their respective spacers. *Id.* at 6:46-49. Step 5 calls for "forming third and fourth spacers ***adjacent the first and second spacers***." *Id.* at 6:50-52. If the third and fourth spacers were formed before the extension region, the third and fourth spacers would block implantation and thus prevent the claimed alignment of the extension regions to the first and second spacers. *See* Part IV.B.3, *infra.*

- Step 5 before Step 6: As discussed below, the third and fourth spacers must be formed before exposing the sides of the gate structure to achieve the express benefit recited in the patent and prosecution history. *See* Part IV.B.3, *infra.*

- Final Steps: Step 5's formation of the third and fourth spacers must necessarily occur before Step 7's "forming source and drain regions … ***aligned to"*** the third and fourth spacers, respectively. *Id.* at 6:55-57. Otherwise, there would be nothing to which the source and drain regions can be aligned. And Step 7 must come after Step 6 to achieve the identified benefit of the patent. *See* Part IV.B.3, *infra.*

Since the steps of independent claim 1 require completion of previous steps, logic and precedent

require that the claimed steps must be performed in the written order.

3. The Practical Reality of the Technology Also Requires Performing the Steps in the Order Written

The practical reality of semiconductor fabrication also calls for the steps to be performed in the order written. Fabricating semiconductors is an incremental process where layer deposition and other fabrication steps build on previous steps, and where "[v]arying the order in which the layers are added yields a physically different device." *Nitride Semiconductors*, 2018 WL 2183270, at *4. The sequence of fabrication steps is thus critical in the '126 patent's technology.

For example, the technology requires that Step 4's formation of extension regions must precede Step 5's formation of the third and fourth spacers. Ex. B ('126 pat.) at 6:46-52. As the patent explains, a function of spacers is to block ion implantation into the portion of the substrate under the spacers, thus providing an "offset" from the gate polysilicon for the doped regions. *See id.* at 1:43-48. If the formation of the third and fourth spacers adjacent the first and second spacers (step 5) preceded the formation of the doped extension regions (Step 4), the third and fourth spacers would block ion implantation into the substrate portion beneath them and would prevent the doped extension regions from being aligned to the first and second spacers as required by claim 1. *Id.* at 6:46-48. To give effect to every word of the claims, Step 4 must precede Step 5.

As another example, "exposing portions of the first and second sides of the gate structure" in Step 6 must occur after forming third and fourth spacers (Step 5) and before forming the source and drain regions (Step 7) in order to achieve the identified benefit of the patent. *Id.* at 6:50-54. As the '126 patent explains, a key problem of the prior art was that spacers on either side of the gate polysilicon limited the formation of silicide on the top surface of the gate structure. *Id.* at 1:53-55. To address this problem, the patent uses multiple spacers of the same material (nitride) so that a single etch step can do two things: (i) etch the blanket silicon nitride layer (126) to form

the outer nitride spacers, and (ii) by being allowed to continue etching, create an overetch of all nitride spacers to expose the sides of the gate polysilicon. *Id.* at 4:55-5:2; *see also id.* at 2:60-65 & 6:14-22. During prosecution, the applicants expressly relied on this benefit to overcome a prior art rejection: "Applicants on the other hand, teach on page 3, lines 30-32, and continuing to page 4, lines 1-2, that a pair of spacers are formed adjacent each side of a gate structure, wherein the spacers are comprised of the same material. ***Because the material of the spacers is the same, they can be recessed using a single etch technique***." Ex. K (Apr. 29, 2004 Amdt.) at 8. Given this emphasis in both the specification and the prosecution, the ability to successively form the outer (third and fourth) spacers and then recess all spacers in the same etch step is critical to the '126 patent. *See Loral Fairchild Corp. v. Sony Corp.*, 181 F.3d 1313, 1325-26 (Fed. Cir. 1999) (relying on teaching in the specification and prosecution history in adopting order of steps).

This critical benefit would not be available if Steps 5 through 7 do not occur in the recited order. If exposing the sides (Step 6) occurred before the formation of the third and fourth spacers (Step 5), two separate etching steps would be necessary: (i) one etching to recede the first and second spacers and expose the top of the gate polysilicon's sides covered by these inner spacers (Step 6), followed by forming the third and fourth spacers (Step 5), and (ii) a second etching to recede these outer spacers and expose portions of the gate polysilicon covered by these additional spacers (Step 6 again). Likewise, if exposing the sides (Step 6) occurred after forming the source and drain (Step 7), two separate etching steps would be required: (i) one etching step to form the third and fourth spacers (Step 5), followed by ion implantation to form the source and drain regions (Step 7), and (ii) then a second etching step to recede all spacers to expose the sides (Step 6). These additional processing steps would preclude the single-etch step benefit that the specification highlighted, and that the applicants relied upon to secure allowance during prosecution.

Because the claims' language, technical realities, and the purpose of the alleged invention all require following the written order of steps, the steps of claim 1 must be performed in the recited sequence. *See Loral*, 181 F.3d at 1321 (construing semiconductor fabrication patent and requiring order of step because, among other things, "the edges of the implantation barrier regions are aligned with the edges of the insulation layer; hence, the insulation layer must already be in place in order to align the barrier regions with it during ion implantation.").

4. The Specification Describes this Sequence of Steps Without Suggesting an Alternative Embodiment

Like the claim language, the specification supports an order of steps requirement. First, the patent describes the method of manufacturing of "the present invention" as a method with the same sequence of steps as in claim 1. Ex. B ('126 pat.) at 2:3-21; *see also id.* at 6:9-22 ("In accordance with the present invention, ... [t]he use of a single etch process to recess the sidewall spacers makes a more robust process and lowers the cost of manufacturing the semiconductor components."). By framing this sequence as its "present invention," the '126 patent requires compliance with the sequence. *Verizon*, 503 F.3d at 1308 ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention.").

Second, the specification's sole embodiment exactly follows claim 1's order of steps, thus indicating its limiting aspect. *Compare* Ex. B ('126 pat.) at 3:21-5:15, *with id.* at cl. 1; *see Respironics, Inc. v. Invacare Corp.*, 303 F. App'x 865, 871 (Fed. Cir. 2008) (requiring order of steps where "the patent's only embodiment" reflected that order).

Third, nowhere in its specification does the patent suggest an alternative ordering of any of these recited steps. *See Loral*, 181 F.3d at 1321 (adopting order of step based, in part, on reasoning that "[n]owhere does the specification suggest implanting the barrier regions prior to growing the insulation layer.").

Fourth, where certain processing steps could be performed out of sequence, the patent expressly noted this fact. Ex. B ('126 pat.) at 5:15-22 ("Although the formation of source/drain extension regions has been described as being formed before the formation of oxide layer 124, it should be understood this is not a limitation of the present invention"). Yet, the patent did not do likewise for the steps recited in claim 1, thus suggesting that the claimed steps must occur in the recited order. Hence, the specification supports an order of step limitation.

In sum, because the intrinsic evidence shows that the steps must be performed in the order written, the Court should construe claim 1 of the '126 patent as requiring the recited order of steps.

C. "adjacent" (cls. 1, 6, 7 of '126 pat.; cls. 1-3, 6 of '620 pat.)

Defendants' Proposed Construction	IFT's Proposed Construction
relatively near and having nothing of the same kind intervening	plain and ordinary meaning

1. A Construction of "Adjacent" Is Necessary

Many of the claims of the '126 and '620 patents use the term "adjacent" to explain a positional relationship between, on one hand, spacers and, on the other hand, either another spacer or the gate polysilicon's side. The parties' dispute about the scope of this term focuses on what its plain and ordinary meaning is. The intrinsic and extrinsic evidence fully supports Defendants' proposal, which comes directly from the term's common meaning. IFT, on the other hand, refuses to articulate what it views as "plain and ordinary meaning," probably to better stretch this term to allow two nitride spacers to be "adjacent" despite having a third spacer of a different material in between them. This argument is tantamount to arguing that Texas is "adjacent" to Mississippi despite having the intervening state of Louisiana and nearly 300 miles in between. In contrast, as the term's common meaning and Defendants' construction contemplates, Louisiana (a state) is adjacent to Texas (a state), despite having the Sabine River (a river) between them. IFT's non-articulated interpretation contradicts the term's plain and ordinary meaning, and will confuse the

jury. As "reliance on a term's 'ordinary' meaning does not resolve the parties' dispute," the Court should resolve the parties' dispute about the claims' scope. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008).

2. The Term's Common Meaning Is Consistent with Defendant's Proposal

The term "adjacent" is not a term of art, and it has a common meaning: "relatively near and having nothing of the same kind intervening." Ex. L (*Websters* 1993) at 26; Ex. M (*Websters* 2002) at 26 (same); *see also* Ex. N (*Merriam-Websters* 1999) ("Adjacent may or may not imply contact but always implies absence of anything of the same kind in between.").

Courts that have considered this term have adopted this common meaning, by excluding intervening structures of the same kind. *E.g.*, *Great Dane Ltd. P'ship v Stoughton Trailers, LLC*, 2009 WL 5200085, at *8 (M.D. Ga. Dec. 23, 2009) ("the Court concludes that 'adjacent' means 'close to or nearby, but not separated by another item of the same type'"); *A to Z Machining Serv., LLC v. Nat'l Storm Shelter, LLC*, 2011 WL 3584716, at *5 (W.D. Okla. Aug. 16, 2011) ("[T]he term 'adjacent' in claim 1 of the '800 Patent is construed as 'not distant: nearby with the absence of anything of the same kind in between.'"); *see also Millipore Corp. v. W.L. Gore & Assocs., Inc.*, 750 F. Supp. 2d 253, 266 (D. Mass. 2010) (construing "adjacent" to mean "next to or adjoining with no intervening structure between the elongate members and the fluid receptacle."). In fact, the Federal Circuit has approved of a construction of "adjacent" that was even narrower than Defendants' proposal. *Boss Indus., Inc., v. Yamaha Motor Corp., U.S.A.*, 333 Fed. App'x 531, 541 (Fed. Cir. 2009) (affirming district court's construction of "adjacent" as "next to or adjoining").

3. The Patents Use "Adjacent" Consistently with Its Common Meaning

The common specification shared by the '126 and '620 patents uses the term consistently with its common meaning in describing the adjacency among nitride spacers and the adjacency

between the gate polysilicon's sides and spacers.

For example, in describing the relationship of the prior art's spacers, the patent sets out the structural adjacency between spacers of different materials exactly as proposed in Defendants' construction. Ex. B ('126 pat.) at 1:41-43 ("***Oxide spacers*** 32 are formed ***adjacent*** sidewalls 22 and ***nitride spacers*** 34 are formed ***adjacent*** oxide spacers 32."), Fig. 1 (showing oxide spacer 32 adjoining sidewall 22, and nitride spacer 34 then adjoining oxide spacer 32). If "adjacent" were as broad as IFT suggests, the patent could have stated that the nitride spacer (34) was adjacent the sidewall (22). Instead, because there is an intervening oxide ***spacer*** (32), the patent indicates that the nitride spacer (34) is adjacent the oxide spacer, which is in turn adjacent the sidewall.

In contrast, the specification describes the nitride spacers as being "adjacent" to the sidewall despite an intervening ***layer*** of oxide (114). Ex. B ('126 pat.) at Abstract ("Successive nitride spacers (118, 128) are formed adjacent the sidewalls of the gate structure (112)."), 2:28-29 ("A pair of spacers are adjacent the first side of the gate structure[.]"), 3:52-54, Fig. 3. Unlike the prior art's oxide spacer (32), this intervening oxide ***layer*** (114) does not preclude adjacency because it is ***not*** an oxide ***spacer***. *Compare id.* at Fig. 3, *with id.* at Fig. 1. In other words, the nitride spacers can be adjacent the sidewalls, because there is no spacer intervening between them.

As another example of how the Luning patents use the term consistently with its common meaning, the specification avoids stating that the outer nitride spacer (128) is adjacent the sidewall, given the intervening inner nitride spacer (118). *Id.* at Fig. 3 (showing location of these spacers). Instead, the specification characterizes these two nitride spacers as a single pair of successive spacers, with the pair being adjacent the gate polysilicon's sides. *Id.* at 2:28-32 (Summary of the Invention reciting "a ***pair of spacers*** are ***adjacent*** the first side of the gate structure" and "a ***pair of spacers*** are ***adjacent*** the second side of the gate structure"). The patents' precise use of

"adjacent" follows the common meaning of this term as captured in defendants' proposal, contrary to IFT's apparent suggestion that "adjacent" allows intervening structures of the same kind in between two "adjacent" structures.

The use of "successive" in describing the nitride spacers in this pair of spacers is also instructive. *See* Ex. B ('126 pat.) at Abstract ("***Successive nitride spacers*** (118, 128) are formed ***adjacent*** the sidewalls of the gate structure (112)."), 6:9-14 ("[T]he amount of polysilicon available for silicide formation is increased by forming ***a succession of spacers*** along each sidewall of the gate conductor, wherein the spacers were formed from the same material."). Because a succession constitutes a sequential grouping, Ex. O (*Websters* 2001) at 1101 (defining "successive" as "[f]ollowing in uninterrupted order or sequence"), the patent's use of "successive" nitride spacers confirms that there is no intervening spacer in this sequence of nitride spacers.

4. The Patents' Stated Benefit Is Consistent with the Common Meaning

The identified benefit of the alleged invention is also consistent with the common meaning of "adjacent." As the specification repeatedly emphasizes, a key advantage of the patent is that the adjacent spacers are made of the same material (nitride) that can be etched in a single processing step to save time and lower manufacturing cost and complexity. Ex. B ('126 pat.) at 4:65-5:2 ("An advantage of spacers 128 and 118 being ***made of the same material***, e.g., silicon nitride, is that they can be recessed using a ***single etch process***, thereby saving time and lowering the cost and complexity of manufacturing the spacers."); *see also id.* at 2:60-62 & 6:14-22 (emphasizing same benefit of using same material for the adjacent spacers).

If IFT were correct that "adjacent" permitted an intervening oxide spacer of any practical thickness between two nitride spacers, the patented technique would not achieve this benefit, because the process for etching of nitride spacers would not be able to etch such an intervening oxide spacer. *See id.* at 3:66-4:4 (discussing different etching chemistry requirement for

selectively etching nitride compared to selectively etching oxide). As a result, additional fabrication steps would be necessary to etch the oxide spacer, thus undercutting the key benefit of lower cost and complexity promised by etching adjacent nitride spacers in a single step.

5. The Prosecution History Contradicts IFT's Strained Position

The prosecution history also calls for the application of Defendants' interpretation of "adjacent." During the prosecution of the '126 patent, original claim 1 did not specify the spacers' materials. Ex. K (Feb. 17, 2004 Resp. to Restriction Req.) at 3. In response to an obviousness rejection of original claim 1, *id.* (Mar. 10, 2004 Non-Final Rejection) at 3-4, the applicants amended their claims to specify that the spacers had to be composed of a "first dielectric material" and argued the importance of a pair of spacers made of the same material: "a ***pair of spacers*** are formed adjacent each side of a gate structure, wherein ***the spacers are comprised of the same material***. Because the material of the spacers is the same, they can be recessed using a single etch technique." *Id.* (May 3, 2004 Amdt.) at 2, 8. Similarly, during the prosecution of the '620 patent, the examiner rejected the original claims as obvious. Ex. P (Jan. 13, 2005 Non-Final Rejection). Trying to distinguish the prior art, the applicants also argued that, in their application, "a ***pair of spacers*** are formed adjacent each side of a gate structure, wherein the ***spacers are comprised of the same material***. Because the material of the spacers are the same, they can be recessed using a single etch technique." *Id*. (Apr. 1, 2005 Amdt.) at 5.

If IFT's position were correct that nitride spacers could still be adjacent despite an intervening spacer of a different material, the nitride spacers would no longer be a pair of spacers. Likewise, if the spacers included other materials beyond nitride (such as silicon oxide), the spacers would no longer be made of the same material. IFT's position is inconsistent with the arguments made during prosecution, and thus cannot be right. In contrast, Defendants' position is in harmony with the prosecution history, and should be adopted. *See Phillips v. AWH Corp.*, 415 F.3d 1303,

1317 (Fed. Cir. 2005) (en banc) ("[T]he prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention.").

V. CLAIM CONSTRUCTION DISPUTE FOR THE '226 PATENT

A. Relevant Technology Background

The '226 patent generally relates to "semiconductor devices comprising transistors exhibition *[sic: exhibiting]* enhanced channel carrier mobility." Ex. D ('226 pat.) at 1:9-10. Before the filing of the '226 patent and as discussed in its Background section, "strained silicon" was a well-known technology used to increase the speed of electron flow in the channel in order to enhance transistor performance. *Id*. at 1:46-51. The '226 patent teaches a semiconductor device that implements this well-known strained silicon technology. Figure 4 of the patent, reproduced below, shows a layer of strained silicon (11) formed on a layer of silicon-germanium (10). *Id*. at 5:2-3 & Fig. 1. A gate electrode (12) is formed over the strained silicon layer, with a gate dielectric layer (13) between the gate electrode and strained silicon. *Id.* at 5:3-6. Spacers (14-15) are then formed on either side of the gate electrode, followed by source and drain regions (17) and then silicide layers (18) on these regions and on top of the gate electrode. *Id.* at 5:6-12. Subsequently, a "conformal stressed nitride liner" (20) is deposited. *Id.* at 5:13-15 & Fig. 2. An optional "conformal silicon oxynitride layer" (30) may also be formed on the stressed nitride liner. *Id.* at 5:15-19 & Fig. 3. A dielectric layer (40) then fills the gaps between the gate electrodes of the transistors on the substrate. *Id.* at 5:23-26 & Fig. 4. Annotated Figure 4 includes annotations and colors for the stressed nitride liner

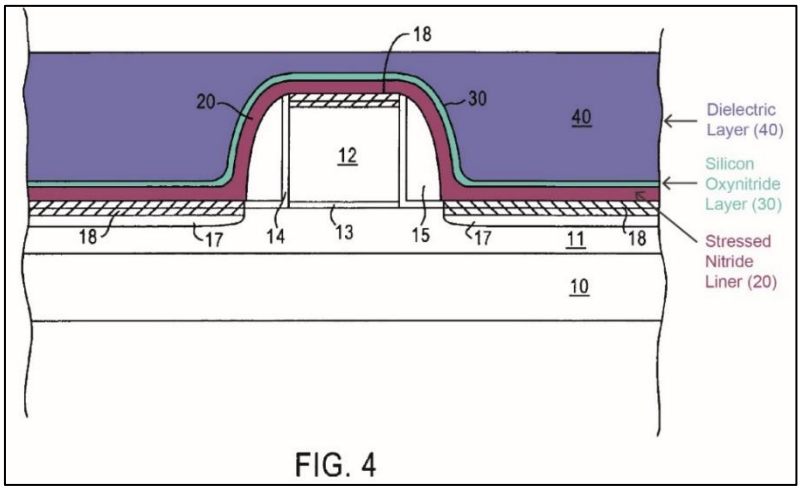


FIG. 4

(20), silicon oxynitride layer (30), and gap-filling dielectric layer (40). *Id.* at Fig. 4 (colors and text labels added).

The '226 patent was filed on July 12, 2004, and issued on March 7, 2006. *Id.* at cover. In mid-July 2020, in response to Defendants' IPR petition against this patent, IFT submitted a statutory disclaimer of claims 1, 3, 4, 5, 6, 8 and 9, leaving only claims 2 and 7 as the surviving claims of the '226 patent. Ex. Q (Jul. 13, 2020 Disclaimer under 37 C.F.R. § 1.321(a)).

B. "conformal" (cls. 1, 2 of '226 pat.)

Defendants' Proposed Construction	IFT's Proposed Construction
having a uniform thickness and following the contours of the layer below	substantially follows the contours of the structure underneath

1. The Parties' Dispute about the Construction Requires Resolution

A construction for this term is necessary because both sides agree as such and have submitted competing proposals for this term. *See O2 Micro*, 521 F.3d at 1360.

The parties concur that "conformal" requires following the contours of the underlying layer or structure, with IFT further introducing the qualifier "substantially" following such contours. IFT's "substantially" qualification is, however, intertwined with the primary dispute regarding this term: whether conformality requires a uniform thickness. Indeed, a layer that only "substantially" follows the contours of the underlying topography necessarily has a non-uniform thickness that prevents the layer from exactly following the contours. Thus, whether "conformal" requires a uniform thickness is the real dispute before the Court.

2. The Intrinsic Evidence Defines "Conformal" as Having Uniform Thickness as It Follows the Underlying Contours

Although the claim language does not resolve this dispute, other intrinsic evidence, which includes the prior art considered during prosecution of the '226 patent, makes clear that the ordinary meaning of "conformal" in this art requires a uniform thickness. *See Philips*, 415 F.3d at

1317 ("The prosecution history, which we have designated as part of the '***intrinsic evidence***,' consists of the complete record of the proceedings before the PTO and ***includes the prior art cited during the examination of the patent***."). Specifically, the patent examiner considered and cited U.S. Patent No. 6,124,217 (the "'217 patent") as a prior art reference during the prosecution of the '226 patent. *See* Ex. D ('226 pat.) at cover; *see also* Ex. R at IFT719_00000533 (Sept. 15, 2005 Notice of Refs. Cited by Examiner). Like Defendants' proposed construction, the '217 patent expressly ties the concept of conformality to having equal thickness as the layer follows the contours of the underlying topography: "Another desired characteristic for interlevel dielectrics used in interconnect formation is ***conformality***, such that ***film thickness is equal over all substrate topography***." Ex. E ('217 pat.) at 2:11-14. As this intrinsic evidence shows, the well-accepted technical meaning of the term requires a uniform thickness as the layer follows the contours of the underlying layer. *See Kumar v. Ovonic Battery Co., Inc.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003) (rejecting district court's construction that disregarded definition provided in prior art reference cited during prosecution, and adopting the definition provided by this prior art); *Arthur A. Collins, Inc. v. N. Telecom Ltd.*, 216 F.3d 1042, 1044-45 (Fed. Cir. 2000) (construing term based on its usage in the prior art cited in the patent).

The definitional statement in the '217 patent is particularly apt here because both the '217 patent and the '226 patent-in-suit share a common inventor (Mr. Sun). Hence, the '217 patent reflects the inventor's understanding of this term. *Compare* Ex. D ('226 pat.) at cover, *with* Ex. E ('217 pat.) at cover; *see Laryngeal Mask Co. Ltd. v. Ambu*, 618 F.3d 1367, 1373 (Fed. Cir. 2010) (construing disputed term based on prior art patents where "[b]oth prior art patents list the same inventor as the patent at issue, Dr. Brain," because "[t]his prior art use of the term would further inform one of skill in the art as to the common meaning of the term backplate").

The ’226 patent itself also reinforces this common understanding of “conformal.” This is most apparent from the ’226 patent’s discussion and depiction of its two “conformal” layers—silicon nitride liner (20) and silicon oxynitride layer (30). *E.g.*, Ex. D (’226 pat.) at 3:19-32, 5:13-18. As depicted in Figure 4, the conformal layers silicon nitride (20, in maroon color) and silicon oxynitride (30, in light teal) follow the contours of the underlying topography while having a uniform thickness throughout. *Id.* at Fig. 4 (colors and labels added). In contrast, the non-conformal dielectric layer (40, in purple) has varying thicknesses depending on the underlying topography. Figure 5 of the patent expands upon this illustration by showing each conformal layer with a uniform thickness as it follows the topography of the transistors, while the thickness of the dielectric layer (40) varies with this topography. *Id.* at Fig. 5. Thus, the ’226 patent’s figures are consistent with the ordinary meaning of “conformal,” and confirm that Defendants’ construction is correct. *See Advanced Steel Recovery, LLC v. X-Body Equipment, Inc.*, 808 F.3d 1313, 1317 (Fed. Cir. 2015) (relying on consistent depiction in drawings to affirm construction); *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1348 (Fed. Cir. 2012) (relying on patent’s figure to adopt narrower construction).

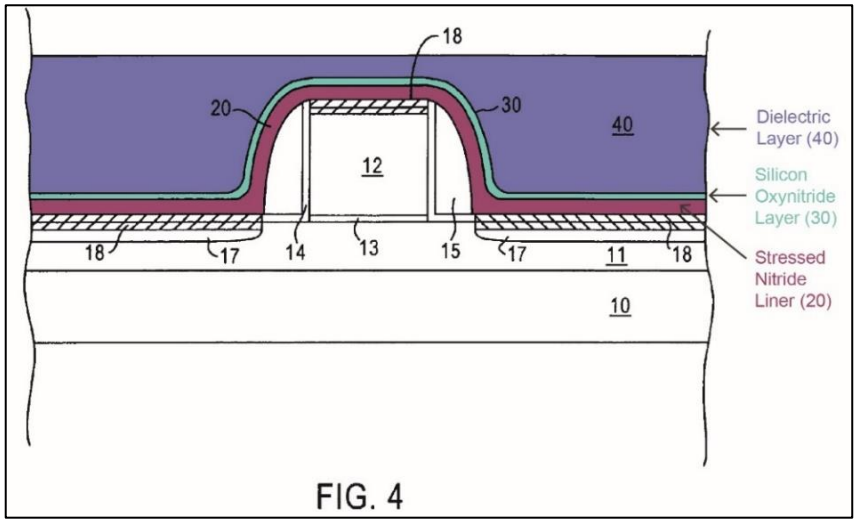


FIG. 4

In sum, the intrinsic evidence uses “conformal” consistently with the term’s ordinary meaning as requiring a uniform thickness. The Court should adopt this ordinary meaning.

3. The Objective Extrinsic Evidence Confirms Defendants’ Construction

In addition to the clear intrinsic evidence, treatises and textbooks on semiconductor

technology published before the filing of the '226 patent expressly recognize that "conformal" requires having a uniform thickness. The following three examples confirm this point.

First, the textbook "*Silicon Processing for the VLSI Era*," published in 2000, provides the following definition for conformal: "*Conformal coverage* is ***defined*** as a condition where ***equal film thickness exists over all substrate topography*** regardless of its slope (i.e., vertical and horizontal surfaces are coated with ***equal film thickness***, Fig. 6-37a)." Ex. S (Wolf & Tauber) at 194 (italics for "Conformal coverage" in original; remaining emphases added). Figure 6-37, discussed in this definition and reproduced in the inset, illustrates the difference between conformal and non-conformal coverage: the conformal film shown in Figure 6-37(a) has equal thickness throughout as the film follows the contours of the underlying layer, while the non-conformal film shown in Figure 6-37(b) has varying thicknesses by being thicker above the trench and then tapering at the bottom of the trench. *Id.* at 195.

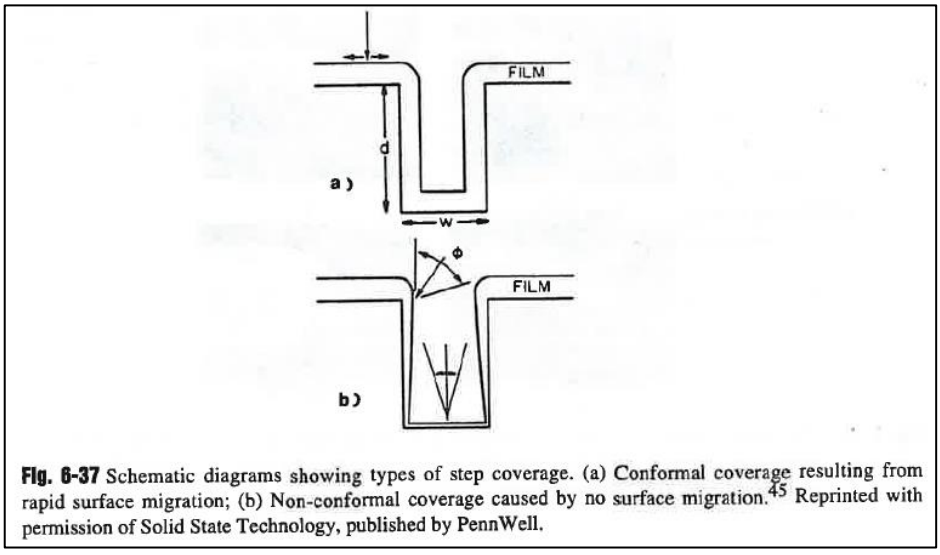


Fig. 6-37 Schematic diagrams showing types of step coverage. (a) Conformal coverage resulting from rapid surface migration; (b) Non-conformal coverage caused by no surface migration.[45] Reprinted with permission of Solid State Technology, published by PennWell.

Second, another treatise, titled "*Semiconductor Manufacturing Technology*" and published in 2001, defines "conformal step coverage" as "***[u]niform material thickness in all regions*** of a wafer surface step, including the sidewalls and corners." Ex. G (Quirk & Serda) at 627. It also provides the illustration below of what qualifies as "conformal" and "non-conformal":

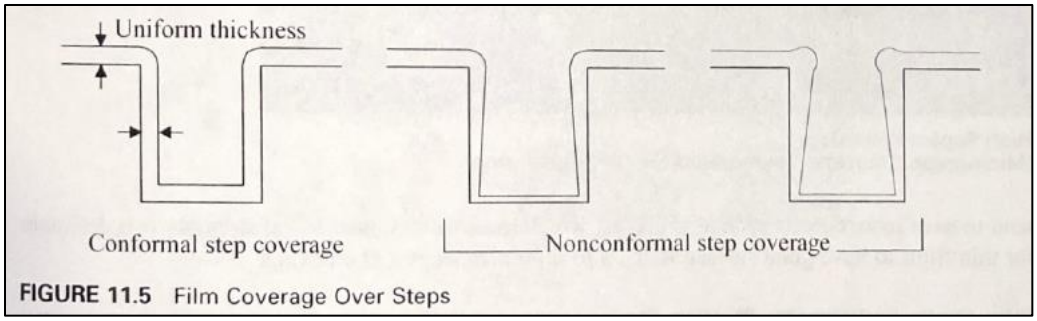


FIGURE 11.5 Film Coverage Over Steps

Id. at 261. As this illustration confirms, a conformal layer has a uniform thickness, while non-conformal films have non-uniform thicknesses at various points.

Third, the "*Semiconductor Glossary*" authored by Professor Jerzy Ruzyllo and published in 2004 (the same year as the '226 patent's application was filed) defines "conformal coating" as a "deposited film which ***thickness remains the same regardless of underlying geometrical features***." Ex. T (Ruzyllo) at 24.

Accordingly, the extrinsic evidence clearly and unambiguously confirms that, contrary to IFT's position, the meaning of "conformal" requires uniform thickness.

VI. INDEFINITENESS FOR LACK OF ANTECEDENT BASIS

A claim is invalid for indefiniteness if its claims, read in light of the specification delineating the patent and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Post-*Nautilus*, a claim can be indefinite if it lacks antecedent basis. *Bushnell Hawthorne, LLC v. Cisco Sys., Inc.*, __ F. App'x __, 2020 WL 2488648, at *3 (Fed. Cir. May 14, 2020). Two terms in the '126 patent are indefinite for lack of antecedent basis.

A. "the portions of the semiconductor material adjacent the gate structure" (cl. 6 of '126 pat.)

Defendants' Proposed Construction	IFT's Proposed Construction
Indefinite for lack of antecedent basis	plain and ordinary meaning

The limitation "***the portions*** of the semiconductor material ***adjacent the gate structure***" in

claim 6 of the '126 patent lacks antecedent basis. Ex. B ('126 pat.) at 7:10-11. The definite article "the" in claim 6 requires an antecedent basis for these portions of semiconductor material adjacent the gate structure. *See* MPEP § 2173.05(e). But there is no prior disclosure of such "portions of the semiconductor material" in claim 6 or in any of the claims from which it depends (claims 1, 2, and 5). In fact, the only "portions" in any of these claims are "***portions*** of the first and second ***sides of the gate structure***" in claim 1. Ex. B ('126 pat.) at 6:53-54; *see also id.* at cls. 2, 5-6. It would defy logic for portions of something "adjacent the gate structure" to refer to portions of the "sides of the gate structure," because a structure cannot be adjacent to itself. This limitation lacks any reasonable clarity. Thus, claim 6 and its dependent claims are indefinite.

B. "the first and second sidewalls" (cl. 8 of the '126 pat.)

Defendants' Proposed Construction	IFT's Proposed Construction
Indefinite for lack of antecedent basis	plain and ordinary meaning

The limitation "***the*** first and second ***sidewalls***" in claim 8 of the '126 patent is indefinite. Ex. B ('126 pat.) at 7:25-26. Although claim 8 depends from a string of claims, *id.* at cls. 1, 2, 5, 6, and 7, none of these prior claims uses the term "sidewalls." In fact, no other claim in the '126 patent uses the term "sidewall" or even "wall." *See generally id.* at 6:34-8:58. IFT cannot try to rescue its indefinite claim by pointing to the term "side" in other claims, because the separately recited terms "side" and "sidewall" must presumptively have different meanings. *See CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG,* 224 F.3d 1308, 1317 (Fed. Cir. 2000) ("In the absence of any evidence to the contrary, we must presume that the use of these different terms in the claims connotes different meanings."). Because there is no reasonable clarity about the antecedent basis of "the … sidewalls," claim 8 is indefinite for this additional reason.

VII. CONCLUSION

Defendants respectfully requests that the Court adopt their proposed constructions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a) on August 5, 2020, and it was served via CM/ECF on all counsel who are deemed to have consented to electronic service. Local Rule CV-5(b)(1).

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